CLAIMS

We claim:

1. A method of providing via for a multilayer semiconductor device, comprising:

   a. providing a first via set on a first layer of a semiconductor device, further comprising:

      i. providing a substantially rectilinear first peripheral border on a first layer of a semiconductor device, an interior of the first peripheral border defining an inner area;

      ii. providing a plurality of first via on the first layer of the semiconductor device within the inner area, the plurality of first via arranged in substantially parallel lines having a predetermined width, each of the plurality of first via having a predetermined separation distance to an adjacent first via; and

   b. providing a second via set on a second layer of a semiconductor device, the second layer disposed above the first layer, the second layer further comprising:

      i. providing the second via set to be substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer; and

      ii. providing a conductive pathway between a predetermined number of the first via of the first via set and those via of the second via set which are disposed substantially parallel to and substantially above the first via of the first via set.

2. The method of claim 1, wherein:

a. each substantially rectilinear first peripheral border is at least one of (i) a rectangle, (ii) a square, or (iii) an octagon; and

b. a maximum distance in a single plane of two opposing sides of the substantially rectilinear first peripheral border of a via set is approximately 70 μm.

3. The method of claim 1, wherein:

a. each side of the substantially rectilinear first peripheral border is approximately 5 μm wide;

b. the predetermined width is approximately 1.5 μm;

c. the predetermined separation distance to an adjacent first via is approximately 1.0 μm; and

d. each of the first via that is substantially parallel and adjacent to a side of the substantially rectilinear first peripheral border is separated from that side by approximately 1 μm.

4. The method of claim 1, wherein:

a. each side of the substantially rectilinear first peripheral border which is substantially parallel to the first via is approximately 5 μm wide;

b. each side of the substantially rectilinear first peripheral border which is substantially perpendicular to the first via comprises an outer edge and an inner edge, each approximately 2 μm wide, the outer edge and the inner edge separated by a separation distance of approximately 0.5 μm;

c. the predetermined width is approximately 12 μm;

d. the predetermined separation distance to an adjacent first via is approximately 2.0 μm; and

e. each via substantially parallel and adjacent to a side of the substantially rectilinear first peripheral border is separated from that side by approximately 10 μm.

5. A multilayer semiconductor device, comprising:

a. a first via set on a first layer of a semiconductor device, further comprising:

i. a substantially rectilinear first peripheral border on a first layer of a semiconductor device, an interior of the first peripheral border defining an inner area;

ii. a plurality of first via on the first layer of a semiconductor device within the inner area, the plurality of first via arranged in substantially parallel lines having a predetermined width, each of the plurality of first via having a predetermined separation distance to an adjacent first via; and

b. a second via set on a second layer of a semiconductor device, the second layer disposed above the first layer, the second via set further comprising:

i. a second via set substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer; and

ii. a conductive pathway between each of the first via of the first via set and each of the first via of the second via set disposed substantially parallel to and substantially above the first via of the first via set; and

c. a pad disposed at a surface of the semiconductor device; and

d. a conductive pathway operatively in communication with at least one of the first via of the first via set and the pad.

6. A multilayer semiconductor device of claim 5, wherein:

a. each substantially rectilinear first peripheral border is at least one of (i) a rectangle, (ii) a square, or (iii) an octagon; and

b. a maximum distance in a single plane of two opposing sides of the substantially rectilinear first peripheral border of a via set is approximately 70 μm.

7. A multilayer semiconductor device of claim 5, wherein:

a. each side of the substantially rectilinear first peripheral border which is substantially parallel to the first via is approximately 5 μm wide;

b. each side of the substantially rectilinear first peripheral border which is substantially perpendicular to the first via comprises an outer edge and an inner edge each approximately 2 μm wide, the outer edge and the inner edge separated by a separation distance of approximately 0.5 μm;

c. the predetermined width is approximately 12 μm;

d. the predetermined separation distance to an adjacent first via is approximately 2.0 μm; and

e. each via substantially parallel and adjacent to a side of the substantially rectilinear first peripheral border is separated from that side by approximately 10 μm.

8. A method of providing via for a multilayer semiconductor device, comprising:

a. providing a first via set on a first layer of a semiconductor device, further comprising:

i. providing a first peripheral border on a first layer of a semiconductor device;

ii. providing a second peripheral border on the first layer, the second peripheral border disposed substantially parallel to the first peripheral border at a predetermined distance, the first peripheral border and the second peripheral border defining an inner area in between the first peripheral border and the second peripheral border; and

iii. providing a plurality of first via on the first layer of a semiconductor device within the inner area, the first via arranged in substantially parallel lines having a predetermined width and a predetermined separation distance to an adjacent first via, the first via disposed substantially perpendicular to the first peripheral border and the second peripheral border; and

b. providing a second via set on a second layer of a semiconductor device, the second layer disposed above the first layer, further comprising:

i. providing a second via set substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer;

ii. providing a conductive pathway between the first peripheral border of the first via set and the first peripheral border of the second via set;

iii. providing a conductive pathway between the second peripheral border of the first via set and the second peripheral border of the second via set; and

iv. providing a conductive pathway between each of the first via of the first via set and each of the first via of the second via set disposed substantially parallel to and substantially above the first via of the first via set.

9. The method of claim 8, further comprising:

a. providing at least one of the first peripheral border or the second peripheral border with a repeating inner design.

10. The method of claim 9, wherein:

a. the repeating inner design comprises a substantially sawtooth pattern.

11. The method of claim 10, wherein:

a. an apex of each tooth of the sawtooth pattern is conductively connected to a nearest co-planar via.

12. The method of claim 9, wherein the repeating inner design further comprises:

a. an outer rectilinear portion; and

b. an inner substantially sawtooth pattern;

c. wherein the conductive pathway of the first peripheral border is disposed proximate the outer rectilinear portion of the first peripheral border and the conductive pathway of the second peripheral border is disposed proximate the outer rectilinear portion of the second peripheral border

13. The method of claim 9, wherein:

a. a distance from an outer edge of the outer rectilinear portion perpendicularly to an apex of a tooth of the sawtooth pattern is approximately 10 μm; and

b. a width of the outer rectilinear portion is approximately 4 μm.

14. The method of claim 8, wherein:

a. each the first peripheral border and the second peripheral border are each approximately 10 μm wide;

b. the inner area is approximately 40 μm wide;

c. the predetermined width is approximately 12 μm.

15. A multilayer semiconductor device, comprising:

a. a first via set on a first layer of a semiconductor device, further comprising:

i. a first peripheral border on a first layer of a semiconductor device;

ii. a second peripheral border on the first layer, the second peripheral border disposed substantially parallel to the first peripheral border at a predetermined distance, the first peripheral border and the second peripheral border defining an inner area in between the first peripheral border and the second peripheral border; and

iii. a plurality of first via on the first layer of a semiconductor device within the inner area, the first via arranged in substantially parallel lines having a predetermined width and a predetermined separation distance to an adjacent first via, the first via disposed substantially perpendicular to the first peripheral border and the second peripheral border; and

b. a second via set on a second layer of a semiconductor device, the second layer disposed above the first layer, further comprising:

i. a via set substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer;

ii. a conductive pathway between the first peripheral border of the first via set and the first peripheral border of the second via set;

iii. a conductive pathway between the second peripheral border of the first via set and the second peripheral border of the second via set; and

iv. a conductive pathway between each of the first via of the first via set and each of the first via of the second via set disposed substantially parallel to and substantially above the first via of the first via set.

16. The multilayer semiconductor device of claim 15, wherein:

a. the first peripheral border and the second peripheral border further comprise a repeating inner design.

17. The multilayer semiconductor device of claim 16, wherein:

a. the repeating inner design comprises a substantially sawtooth pattern.

18. A method of providing via for a multilayer semiconductor device, comprising:

a. providing a first via set on a first layer of a semiconductor device, further comprising:

i. providing a first peripheral border on the first layer of a semiconductor device;

ii. providing a second peripheral border on the first layer of a semiconductor device, the second peripheral border disposed substantially parallel to the first peripheral border, the second peripheral border further disposed at a distance defining an inner area in between the first peripheral border and the second peripheral border;

iii. providing a first inner border disposed in the inner area substantially parallel to the first peripheral border at a predetermined separation distance;

iv. providing a second inner border disposed in the inner area substantially parallel to the second peripheral border at the predetermined separation distance;

v. providing a third inner border disposed in the inner area substantially parallel to the first inner border at a predetermined separation distance;

vi. providing a fourth inner border disposed in the inner area substantially parallel to the second inner border at the predetermined separation distance; and

vii. providing a first via on the first layer of a semiconductor device within the inner area in between the second inner border and the fourth inner border at a predetermined separation distance from the third inner border and the fourth inner border; and

b. providing a second via set on a second layer of a semiconductor device, the second layer disposed above the first layer, further comprising:

i. providing a second via set substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer;

ii. providing a conductive pathway between the first inner border of the first via set and the first inner border of the second via set;

iii. providing a conductive pathway between the third inner border of the first via set and the third inner border of the second via set; and

iv. providing a conductive pathway between the first via of the first via set and the first via of the second via set.

19. The method of claim 18, wherein:

a. the first peripheral border and the second peripheral border are each approximately 5 μm wide;

b. a distance from an outer edge of the first peripheral border perpendicularly to a furthest distance on an outer edge of the second peripheral border is approximately 70 μm;

c. the first inner border and the second inner border are each approximately 2 μm wide;

d. the third inner border and the fourth inner border are each approximately 2 μm wide;

e. the first inner border is separated from each of the first peripheral border and the third inner border by approximately 2 μm;

f. the third inner border is separated from each of the second peripheral border and the fourth inner border by approximately 2 μm;

g. the third inner border and the fourth inner border are separated from the inner area by approximately 2 μm; and

h. the inner area is a rectangle approximately 30 μm wide and 60 μm long.

20. The method of claim 19, wherein:

a. the first peripheral border is longer than the first inner border;

b. the first inner border is longer than the third inner border;

c. the second peripheral border is longer than the second inner border; and

d. the second inner border is longer than the fourth inner border.

21. The method of claim 20, wherein:

a. the first peripheral border is substantially the same length as the second peripheral border;

b. the first inner border is substantially the same length as the second inner border; and

c. the third inner border is substantially the same length as the fourth inner border.

22. A multilayer semiconductor device, comprising:

a. a first via set on a first layer of a semiconductor device, further comprising:

i. a first peripheral border on the first layer of a semiconductor device;

ii. a second peripheral border on the first layer of a semiconductor device, the second peripheral border disposed substantially parallel to the first peripheral border, the second peripheral border further disposed at a distance defining an inner area;

iii. a first inner border disposed in the inner area substantially parallel to the first peripheral border at a predetermined separation distance;

iv. a second inner border disposed in the inner area substantially parallel to the second peripheral border at the predetermined separation distance;

v. a third inner border disposed in the inner area substantially parallel to the first inner border at a predetermined separation distance;

vi. a fourth inner border disposed in the inner area substantially parallel to the second inner border at the predetermined separation distance; and

vii. a first via on the first layer of a semiconductor device within the inner area in between the second inner border and the fourth inner border at a predetermined separation distance from the third inner border and the fourth inner border; and

b. a second via set on a second layer of a semiconductor device, the second layer disposed above the first layer, further comprising:

i. a via set substantially identical to the first via set, the second via set disposed substantially parallel to the first via set in a plane defined by the second layer;

ii. a conductive pathway between the first inner border of the first via set and the first inner border of the second via set;

iii. a conductive pathway between the third inner border of the first via set and the third inner border of the second via set; and

iv. a conductive pathway between the first via of the first via set and the first via of the second via set.

23. The multilayer semiconductor device of claim 22, wherein:

a. the first peripheral border and the second peripheral border are each approximately 5 μm wide;

b. a distance from an outer edge of the first peripheral border perpendicularly to a furthest distance on an outer edge of the second peripheral border is approximately 70 μm;

c. the first inner border and the second inner border are each approximately 2 μm wide;

d. the third inner border and the fourth inner border are each approximately 2 μm wide;

e. the first inner border is separated from each of the first peripheral border and the third inner border by approximately 2 μm;

f. the third inner border is separated from each of the second peripheral border and the fourth inner border by approximately 2 μm;

g. the third inner border and the fourth inner border are separated from the inner area by approximately 2 μm; and

h. the inner area is a rectangle approximately 30 μm wide and 60 μm long.

24. The semiconductor device of claim 22, wherein:

a. the first peripheral border is longer than the first inner border;

b. the first inner border is longer than the third inner border;

c. the second peripheral border is longer than the second inner border; and

d. the second inner border is longer than the fourth inner border.

25. The semiconductor device of claim 22, wherein:

a. the first peripheral border is substantially the same length as the second peripheral border;

b. the first inner border is substantially the same length as the second inner border; and

c. the third inner border is substantially the same length as the fourth inner border.